Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1.A method for PCI (Peripheral Component Interconnect) Express PM (Power Management) using a PCI PM mechanism in a computer system, the computer system including a PCI PME (Power Management Event) controller and a PCI Express Root Complex, the method comprising:

converting a Beacon signal generated by the PCI Express Root Complex into a Pseudo-PME signal, the Beacon signal asserting the Pseudo-PME signal so that a voltage of Pseudo-PME signal changes from a first level to a second level;

providing a Pseudo-PME line electrically connecting an output of the PCI Express Root Complex with a PME input of the PCI PME controller for transmitting the Pseudo-PME signal to the PCI PME controller, the PME input receiving PME signals generated by PCI-compliant devices through a PCI Bus of the computer system; and

before the computer system is under the control of an operating system, de-asserting the Pseudo-PME signal so that the voltage of the Pseudo-PME signal changes from the second level to the first level;

wherein the first level and the second level of the voltage

of the Pseudo-PME signal are PCI-compliant.

[c2] 2.The method of claim 1 wherein the PCI PME controller is a chipset of the computer system.

[c3] 3.The method of claim 1 further comprising providing a sequential circuit to convert the Beacon signal into the Pseudo-PME signal.

[c4] 4.The method of claim 3 wherein the sequential circuit is a latch or a flip flop.

[c5] 5.The method of claim 1 further comprising providing a timer to control the time interval between asserting and de-asserting the Pseudo-PME signal.

[c6] 6.The method of claim 1 further comprising converting a pulse of the Beacon signal into a lower frequency pulse to control a time interval between asserting and de-asserting the Pseudo-PME signal.

[c7] 7.The method of claim 6 further comprising providing a synchronizer to convert the pulse of the Beacon signal into the lower frequency pulse.

[c8] 8.The method of claim 6 wherein the lower frequency pulse is an active-low pulse and functions as the Pseudo-PME signal in the computer system.

[c9] 9.The method of claim 1 further comprising utilizing a main power recovery related signal to control a time interval between asserting and de-asserting the Pseudo-PME signal.

[c10] 10.The method of claim 9 wherein the main power recovery related signal is a PWROK signal of the computer system.

[c11] 11.The method of claim 9 wherein the main power recovery related signal is a PSON signal of the computer system.

[c12] 12.The method of claim 9 wherein the main power recovery related signal is an RST signal of the computer system.

[c13] 13.The method of claim 9 wherein the main power recovery related signal is a BIOS (Basic Input Output System) driven signal of the computer system.

[c14] 14.The method of claim 1 wherein the PCI PME controller includes an event register which can be set by the PCI PME controller when the Pseudo-PME signal is asserted but cannot be cleared when the Pseudo-PME signal is de-asserted, the method further comprising clearing the event register with computer code resident in a memory of the computer system.

[c15] 15.The method of claim 14 wherein the computer code is a device driver of the computer system.

[c16] 16. A computer system comprising:
a PCI PME controller having a PME input;
a PCI Express Root Complex having an output for outputting a generatedBeacon signal;
a sequential circuit electrically connected to the output of PCI Express Root Complex, the sequential circuit having an output for outputting a Pseudo-PME signal of a first voltage level or a second voltage level according to the Beacon signal; and
a Pseudo-PME line electrically connecting theoutput of the sequential circuitto the PME input of the PCI PME controller;
wherein the firstvoltage level and the secondvoltage level are PCI-compliant.

[c17] 17. The computer system of claim 16 wherein when the sequential circuit inputs a Beacon signal from the PCI Express Root Complex, the Pseudo-PME signal is changed from the first voltage level to the second voltage level.

[c18] 18. The computer system of claim 17 further comprising a timer connected to the sequential circuit to control when the Pseudo-PME signal is changed from thesec-

ondvoltage level to thefirstvoltage level.

[c19] 19. The computer system of claim 17 wherein a main power recovery related signal is utilized to control when the Pseudo-PME signal is changed from thesecondvoltage level to thefirstvoltage level.

[c20] 20. The computer system of claim 17 wherein the PCI PME controller further comprises an event register, the event registerbeing set when the Pseudo-PME signal is changed from thefirstvoltage level to thesecondvoltage level, and the computer system further comprises a memory comprising computer code executed by the computer system when the Pseudo-PME signal changes from the secondvoltage level to the firstvoltage level, the computer code clearing the event register.